

GA-M68MT-S2

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05	PROCESSOR DDR INTERFACE	
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11	MCP61-DAC, RGMII	
12	MCP61-PCI	
13	MCP61-SATA, IDE	
14	MCP61-USB, HD-Audio, GPIO	
15	MCP61-Power, Gnd	
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17	PCI SLOT COM,LPT	
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22	POWER SEQ	
23	ATX, VCC12_DUAL, VDDA25 F_PANEL	
24	DDR POWER	
25	PWM ISL6324A	

[illegible]

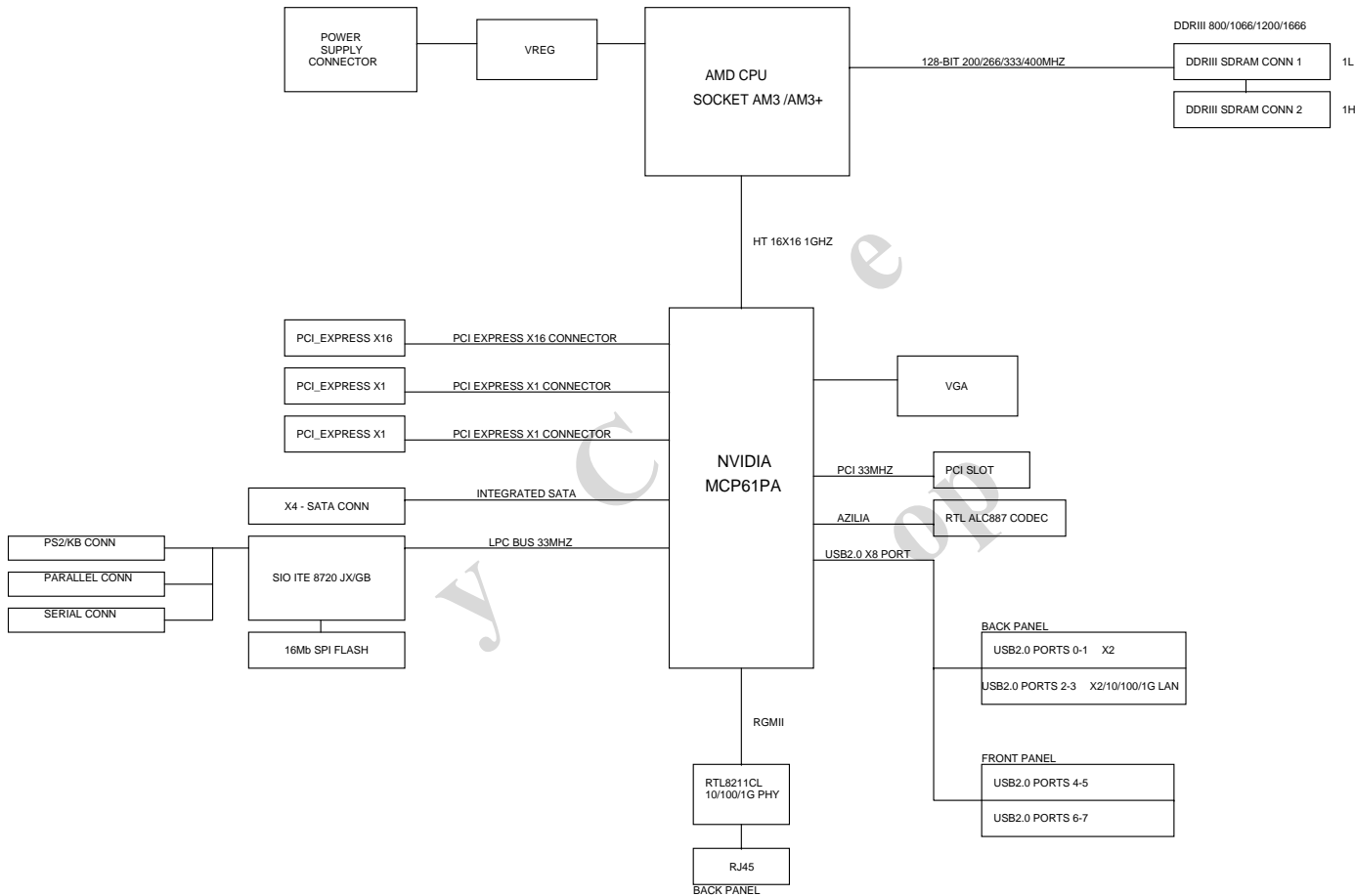
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Title			
BLOCK DIAGRAM			
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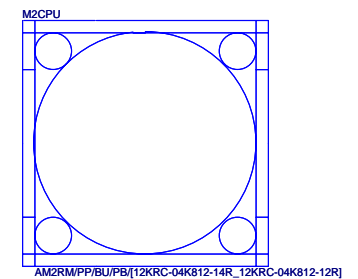
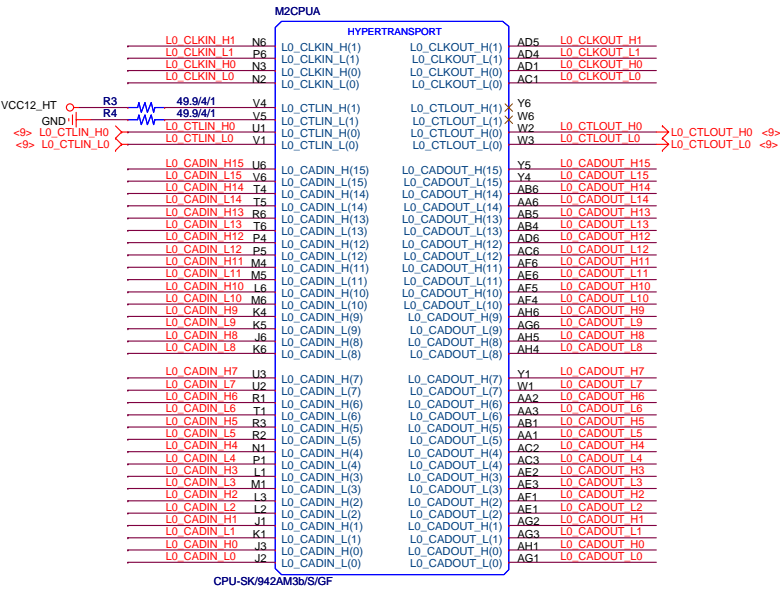
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BOM & PCB MODIFY HISTORY				
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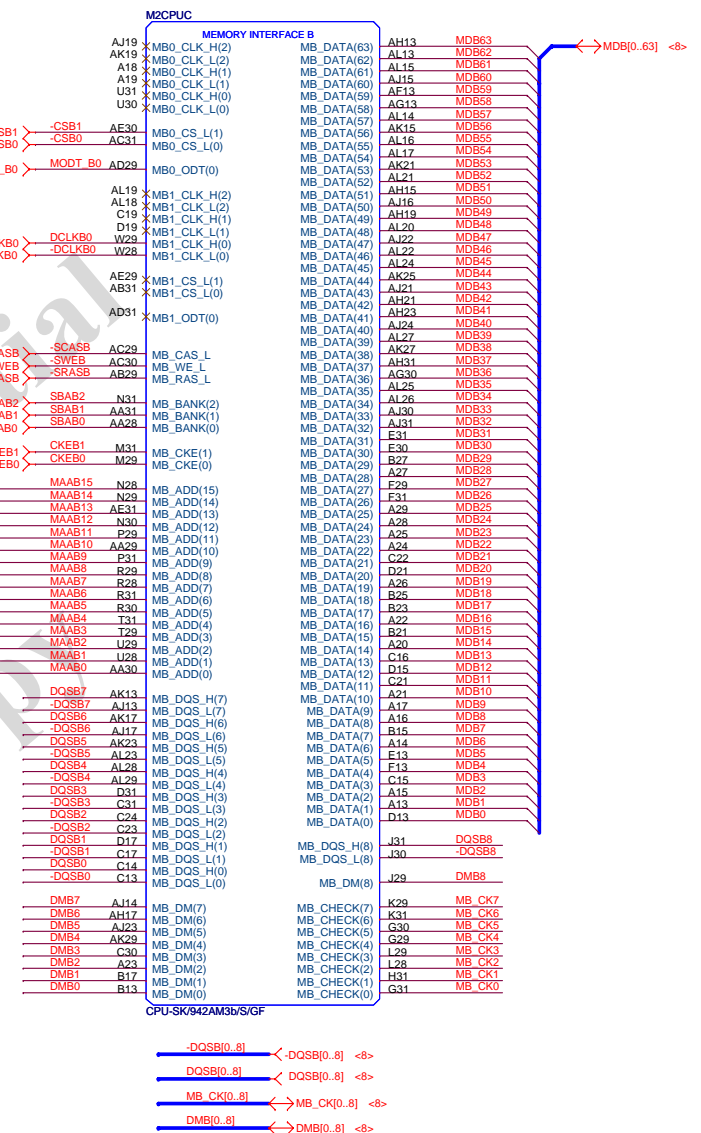
BLOCK DIAGRAM

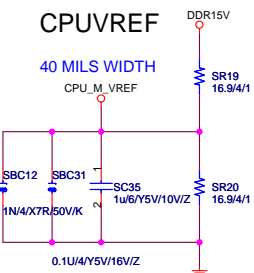
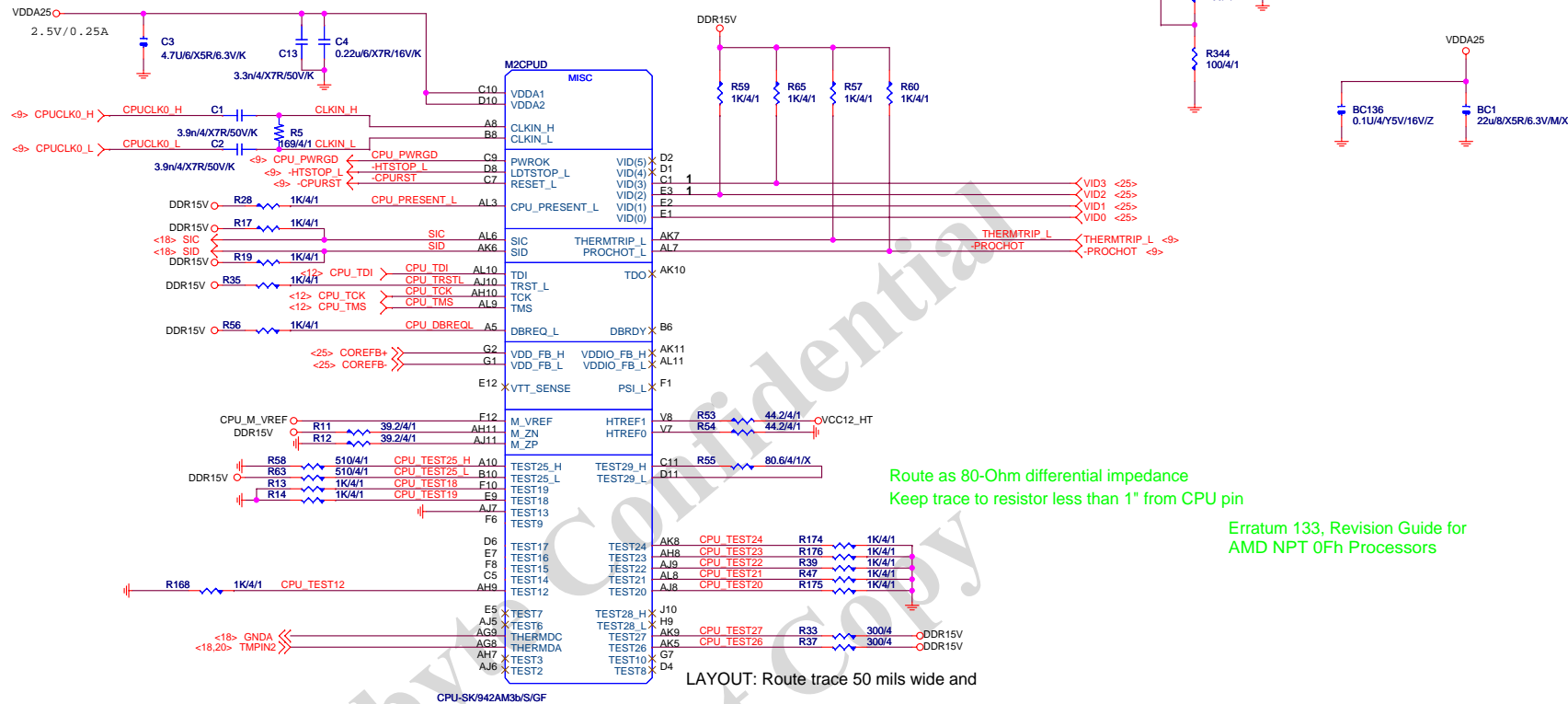
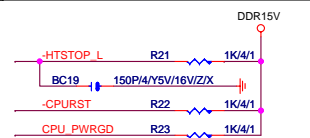


CPU_VDD_RUN = VCORE
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VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

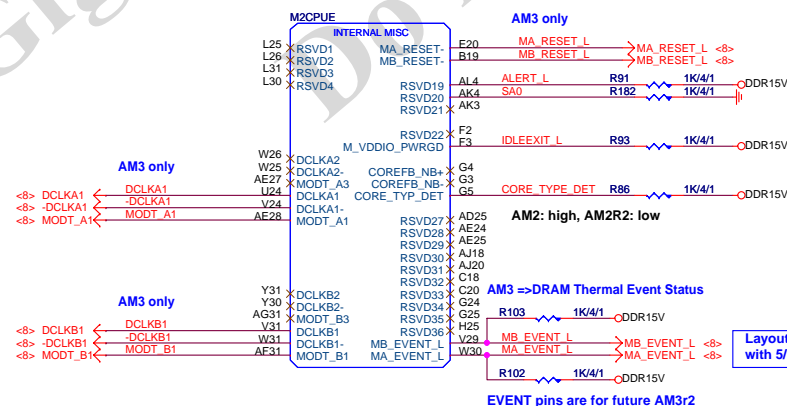
VLDT_A = VCC12_HT
VLDT_B = HT12B



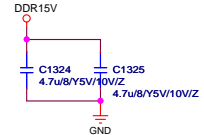
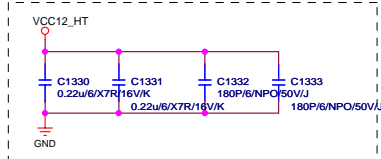
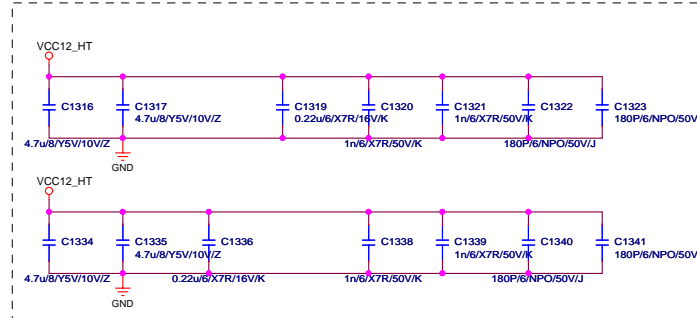
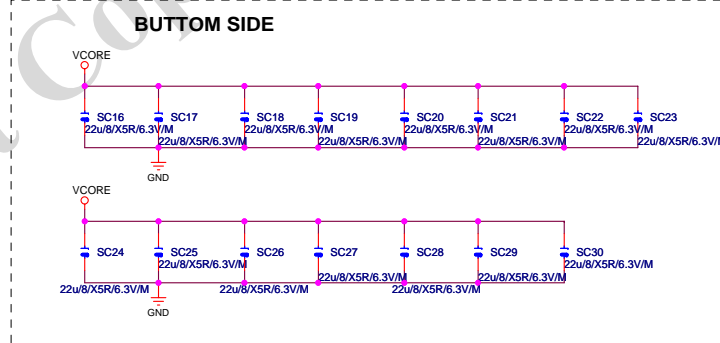
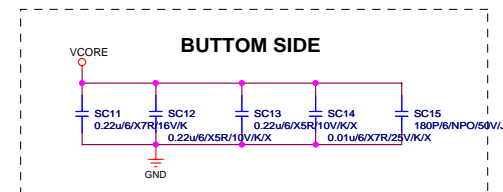
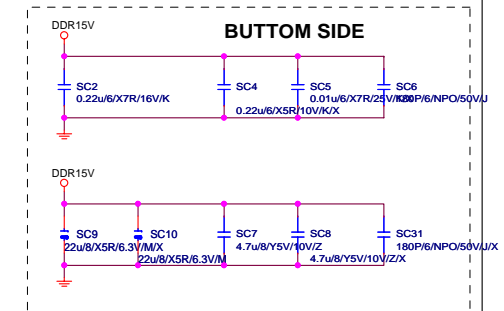
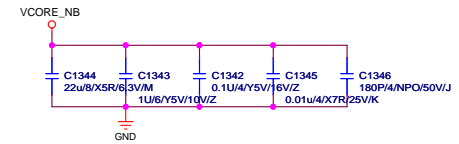
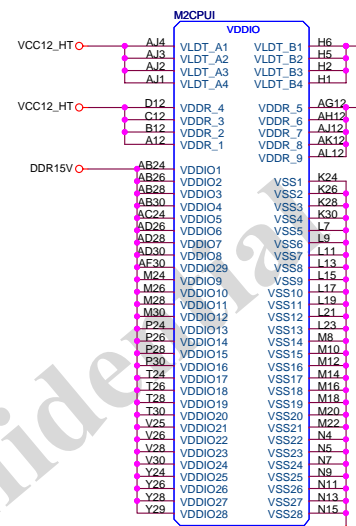
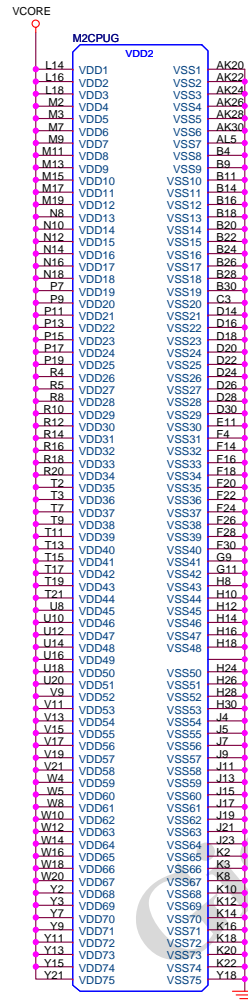


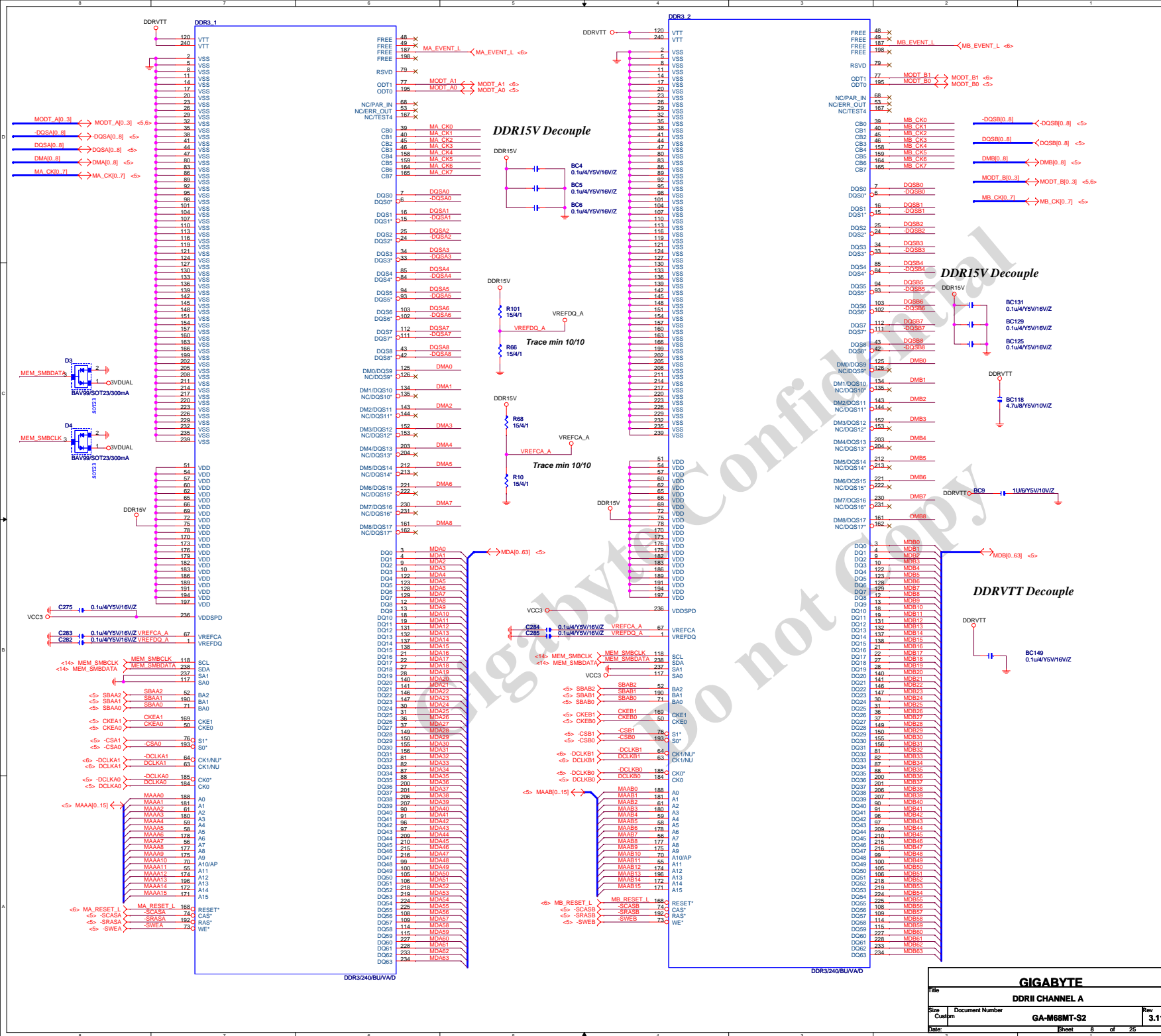


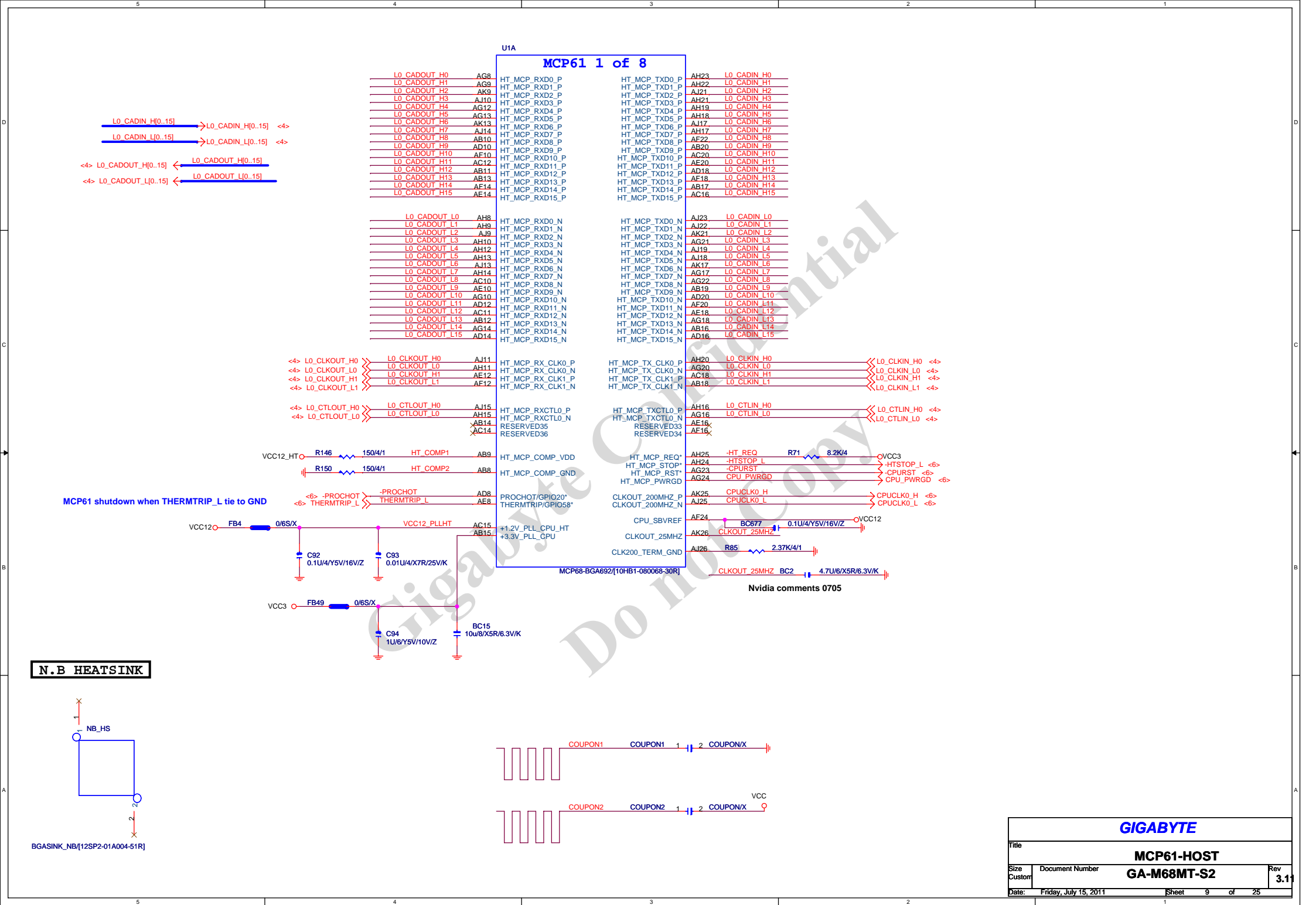
LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

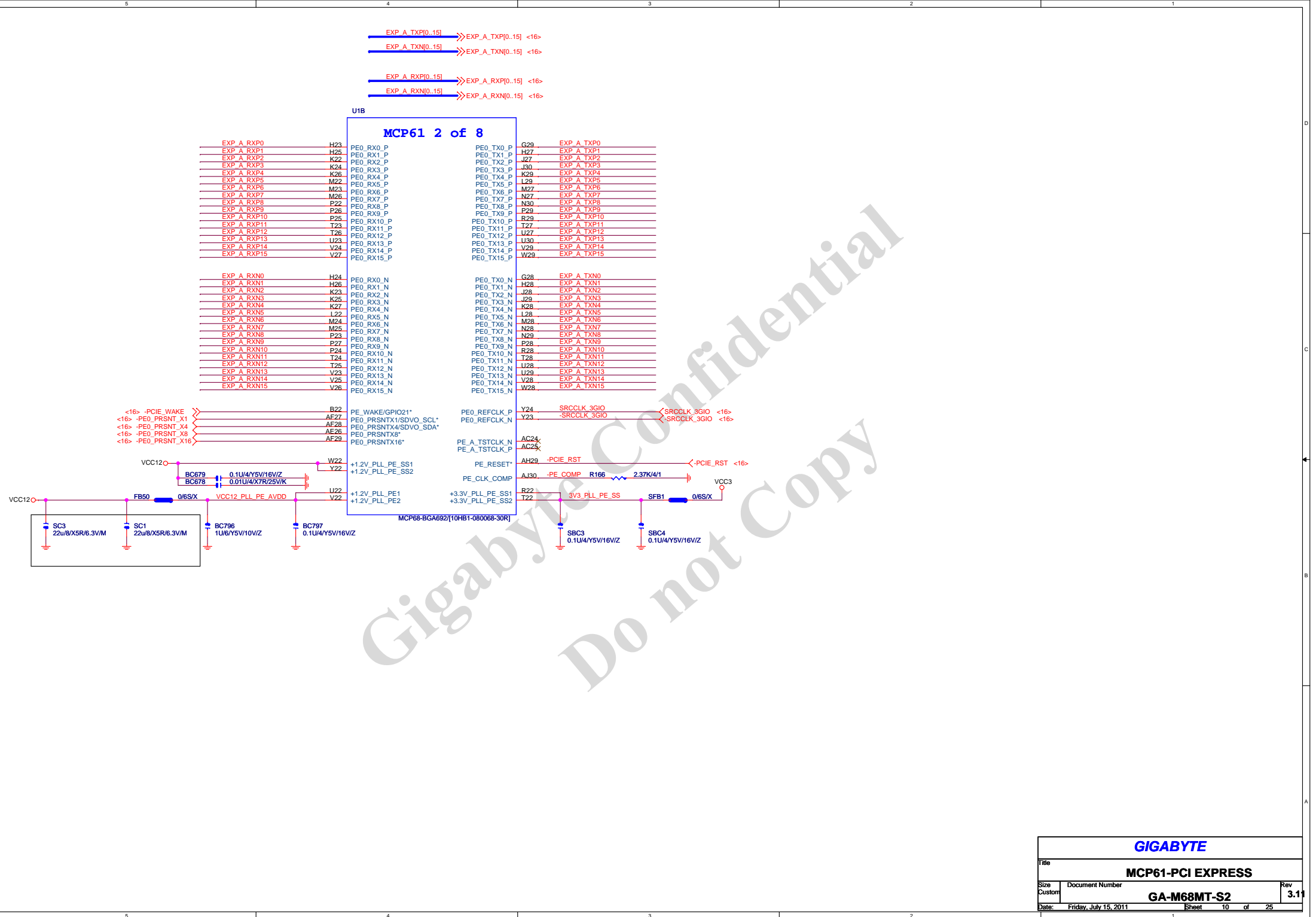


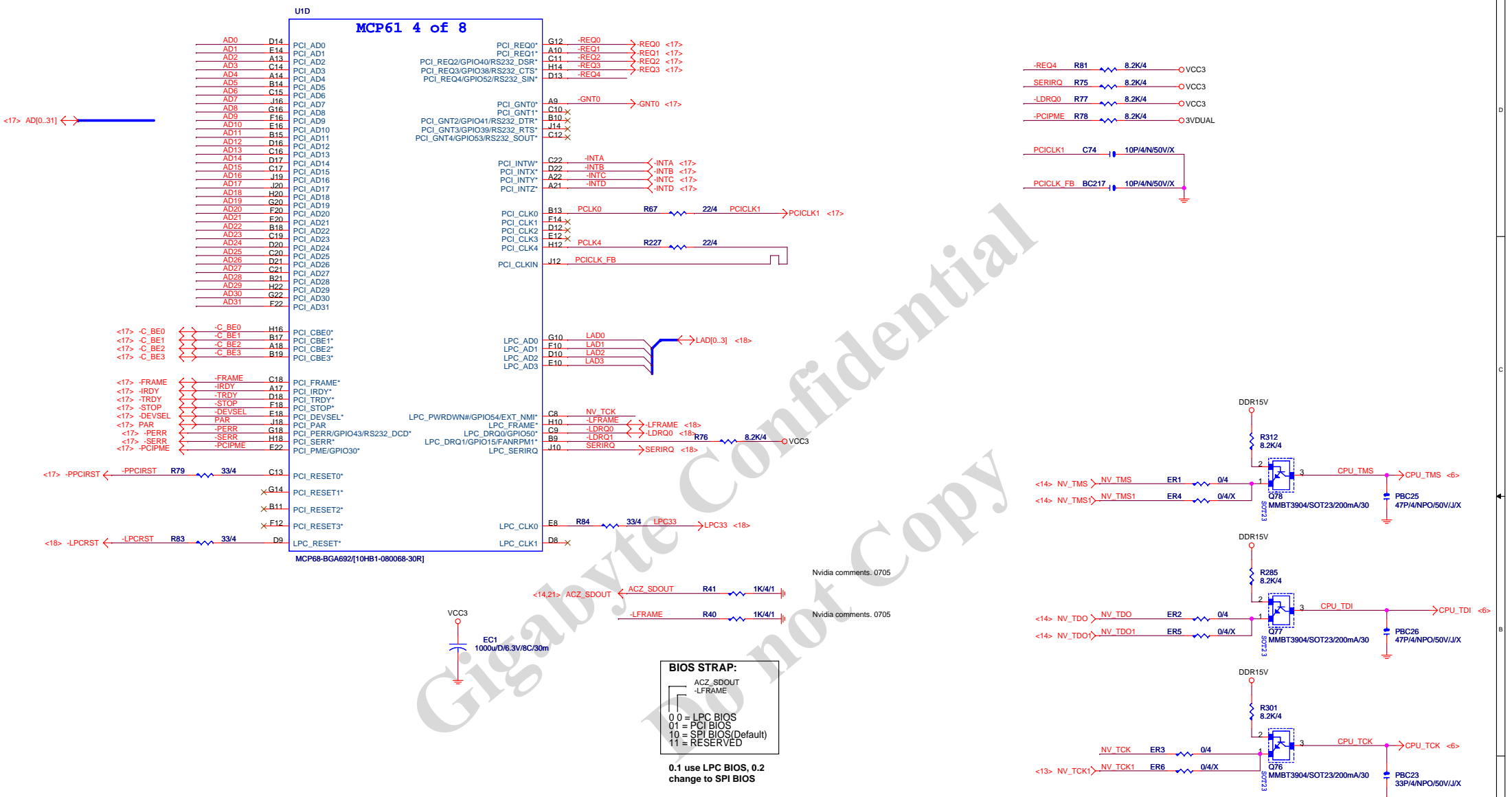
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CPU CONTROL		
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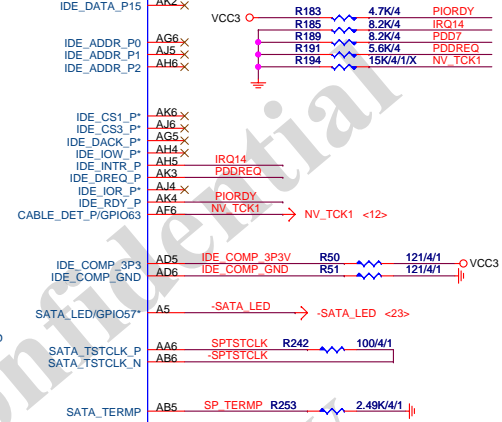
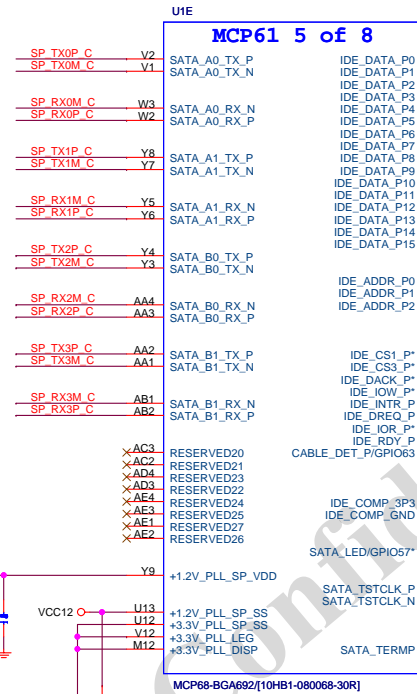
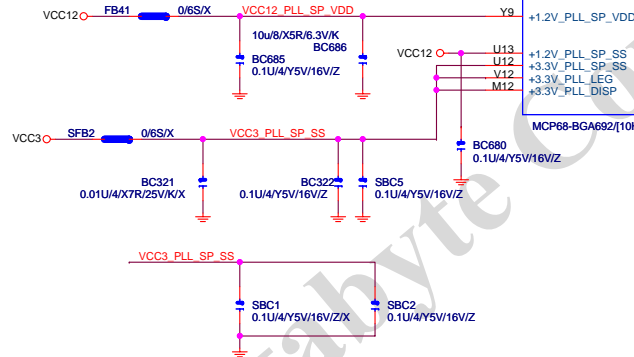
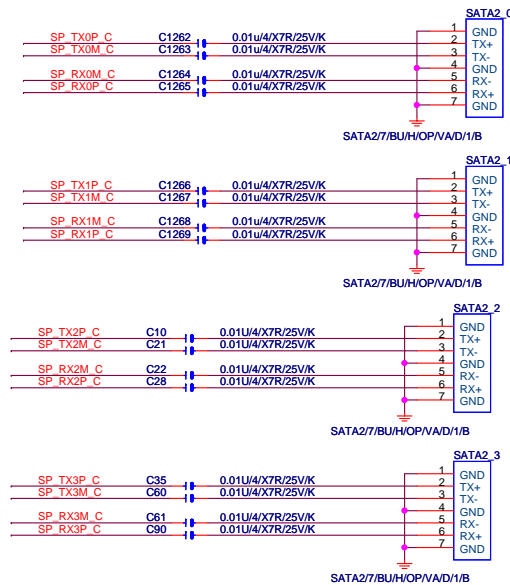


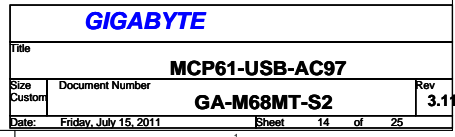


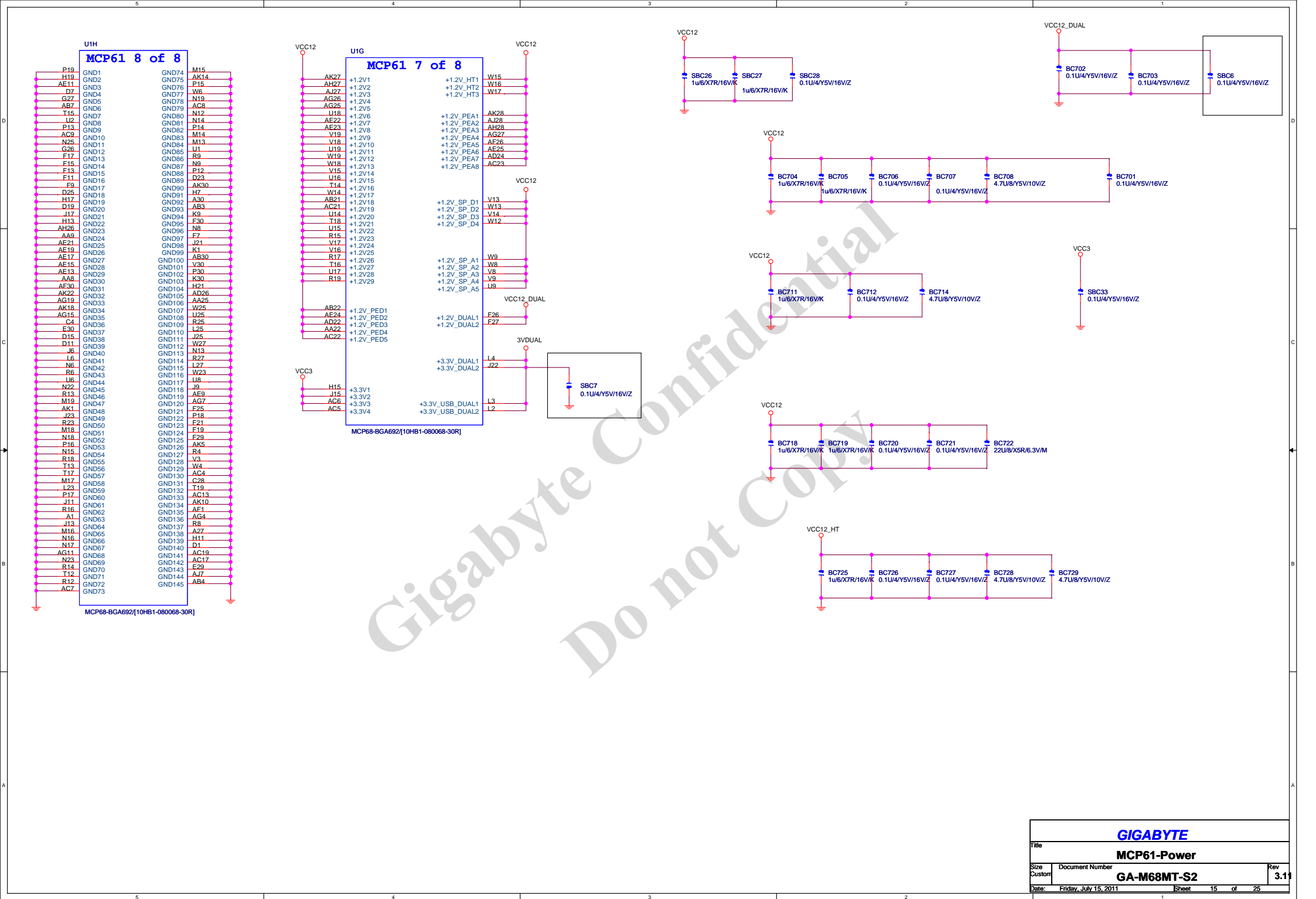


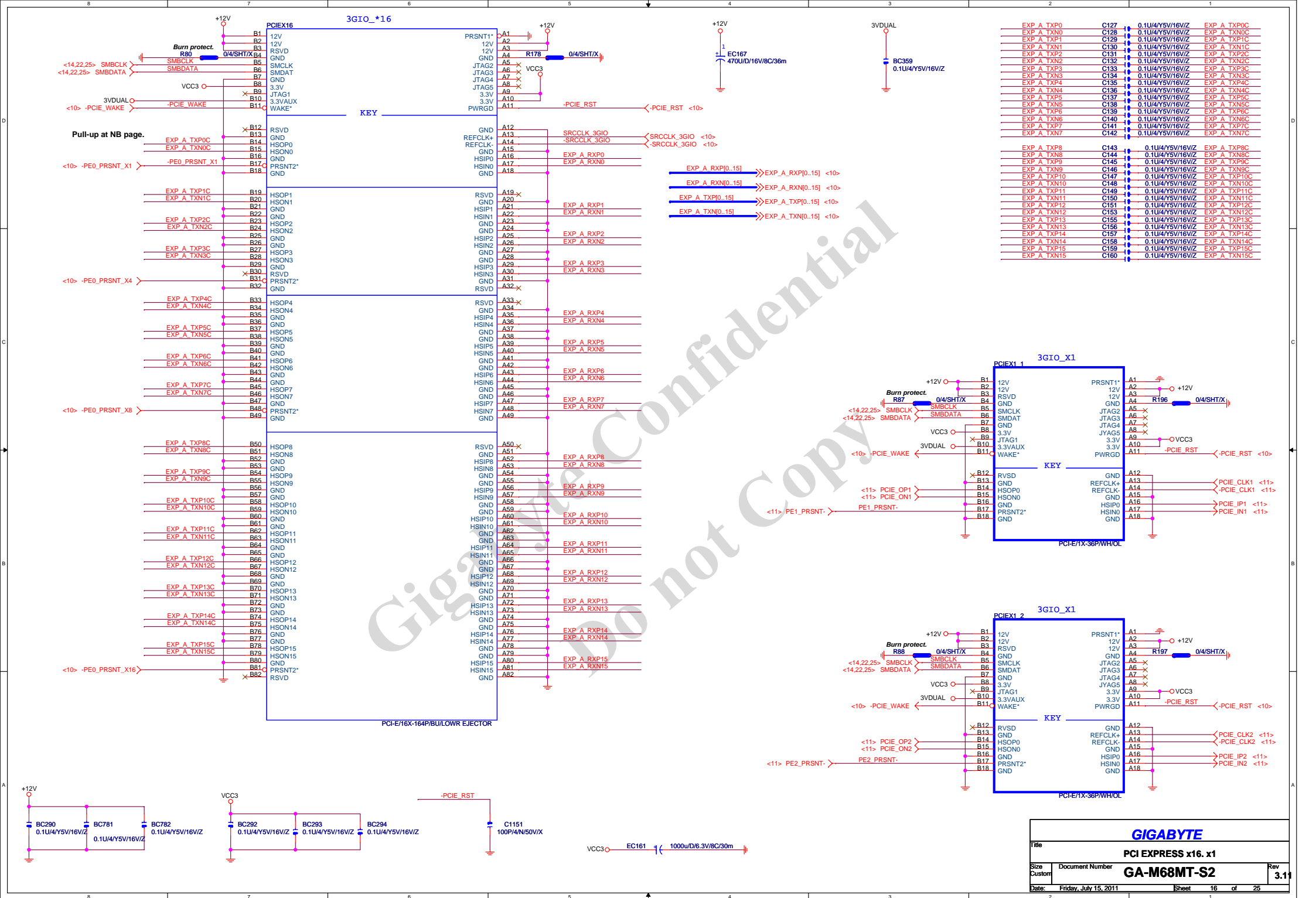




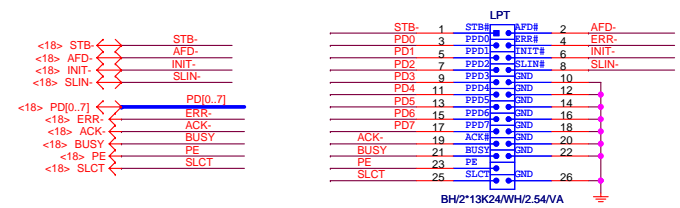
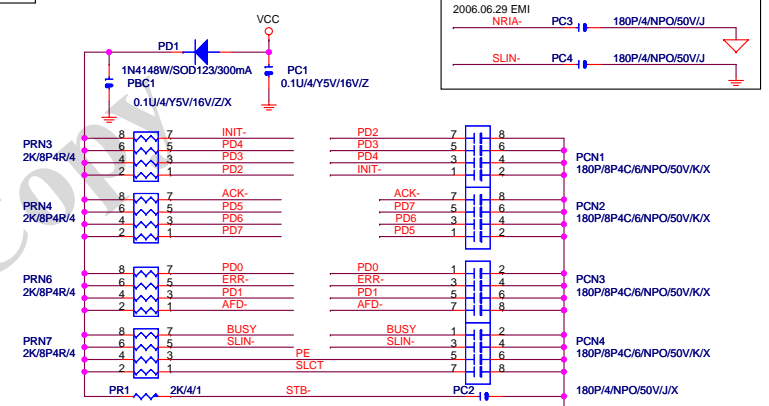
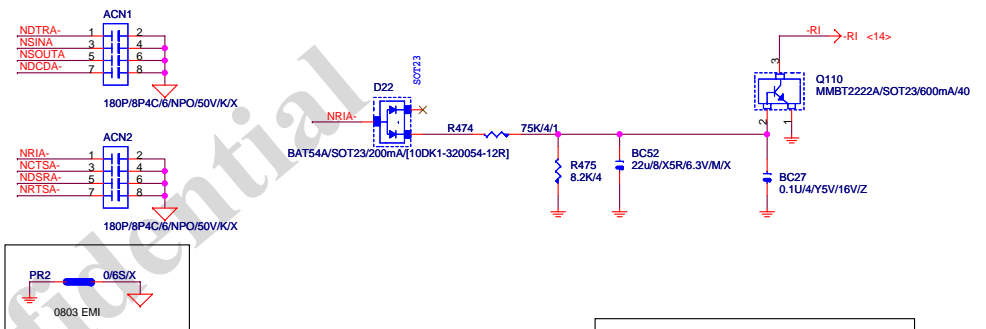
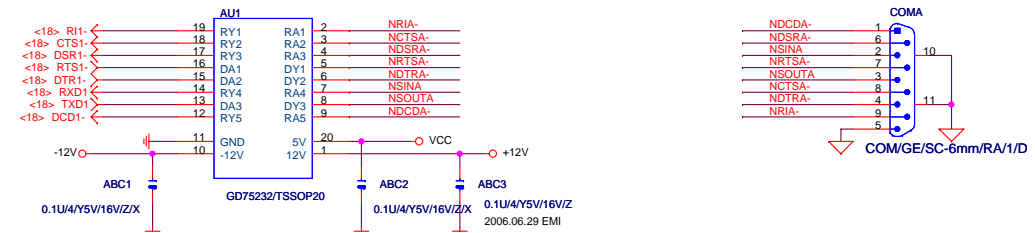
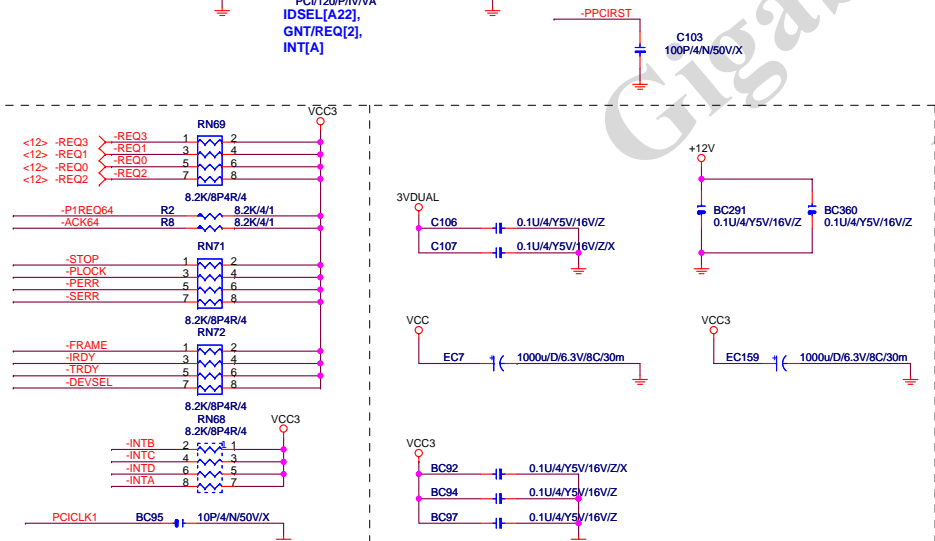
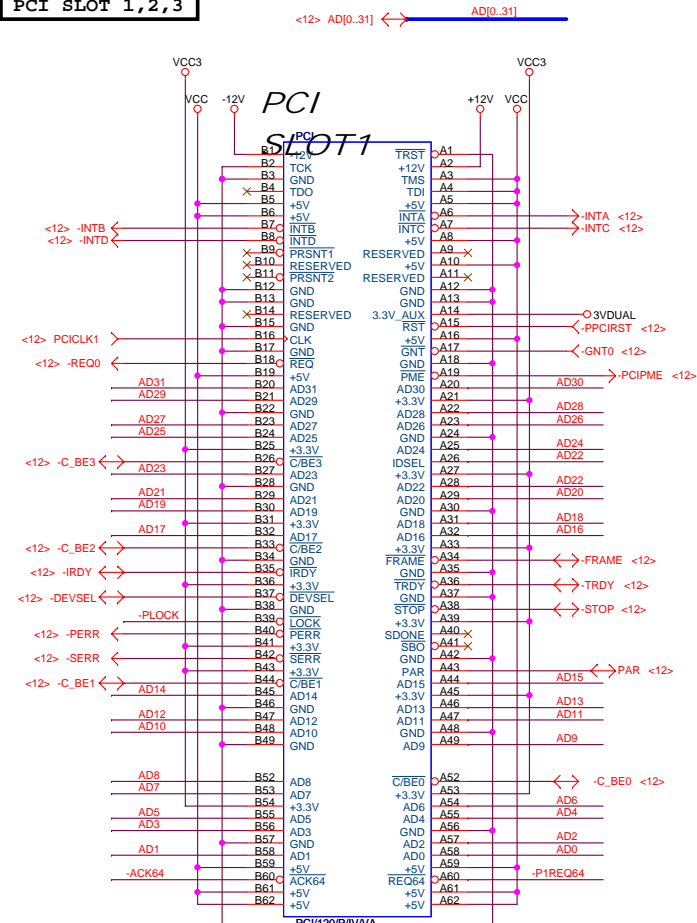


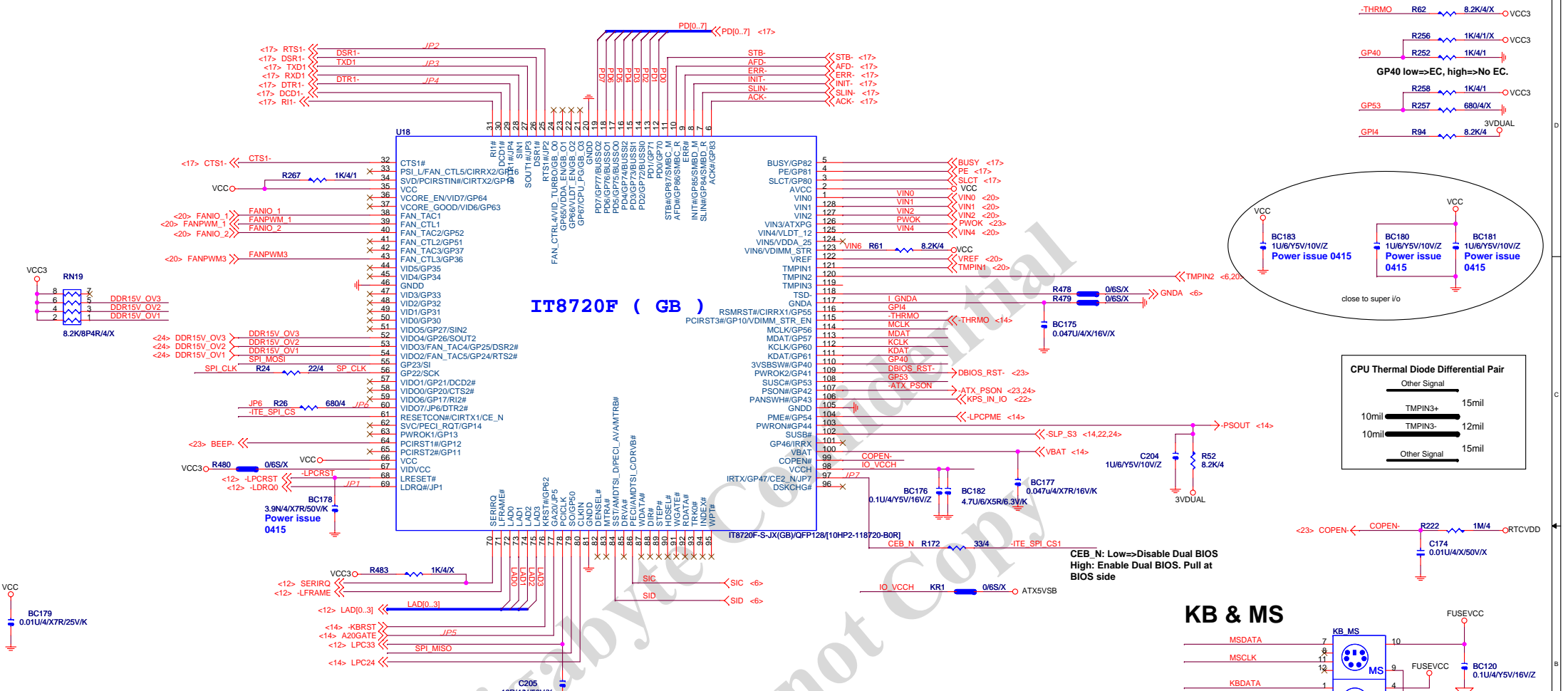






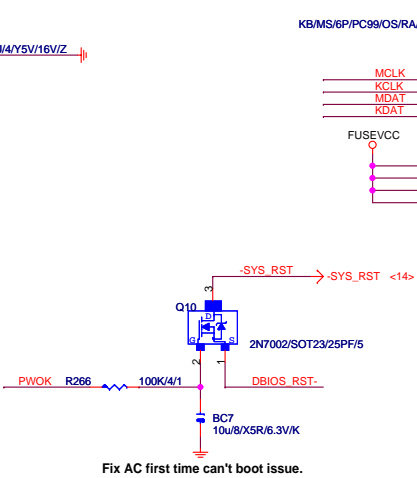
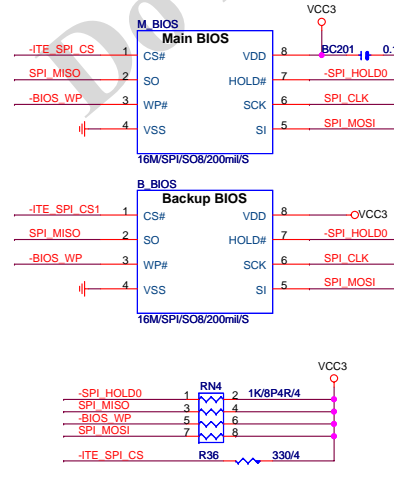
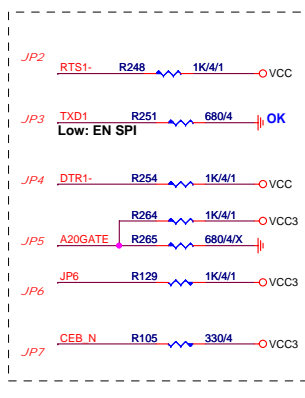
PCI SLOT 1,2,3





IT8720GB Power On Strapping Options				
	Symbol	value	Description	
JP2	VIDO_EN	1	Disable VID output pins	
Pin 25		0	Enable VID output pins	
JP3	CHIP_SEL		Chip selection in Configuration	
Pin 27				
JP4	K8PWR_EN	1	K8 power sequence disabled	
Pin 29		0	K8 power sequence enabled	
JP3 & JP5	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h	
Pin 27 & Pin 77		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh	
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h	
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h	
JP5	WDT_EN	1	Disable WDT to rest PWROK	
Pin 77		0	Enable WDT to rest PWROK	
JP6	SVID_EN	1	Disable SVID Function	
Pin 60		0	Enable SVID Function	
JP7	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only	
Pin 97		0	Disable Dual BIOS Function for GigaByte Only	

IT8720CX->FX(and later) strapping change.
JP1 no use, JP3 change to Low.



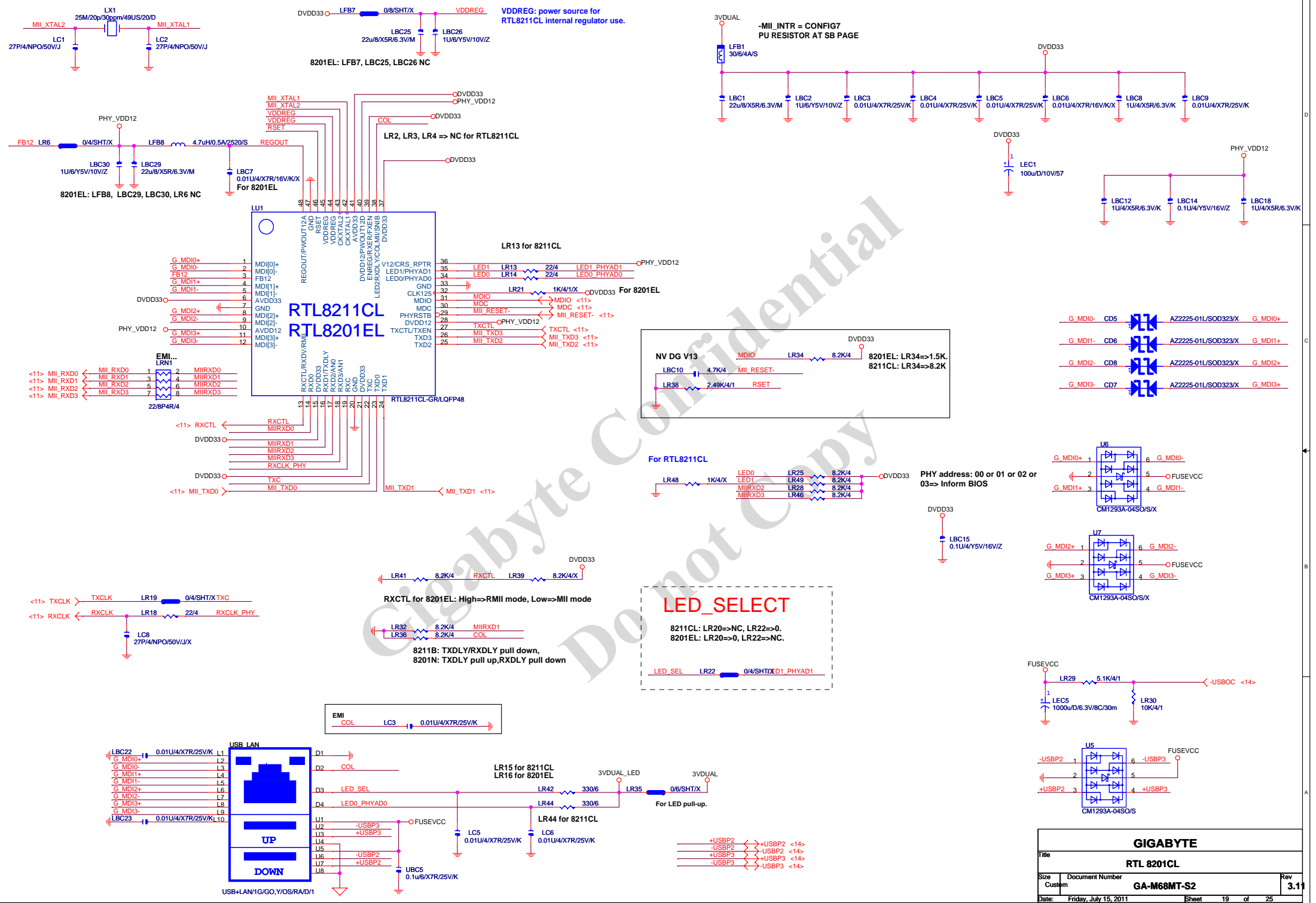
KB & MS

KB/MS/6P/PC99/OS/RA/D2/[11NR6-802006-19R_11NR6-802006-1ER]

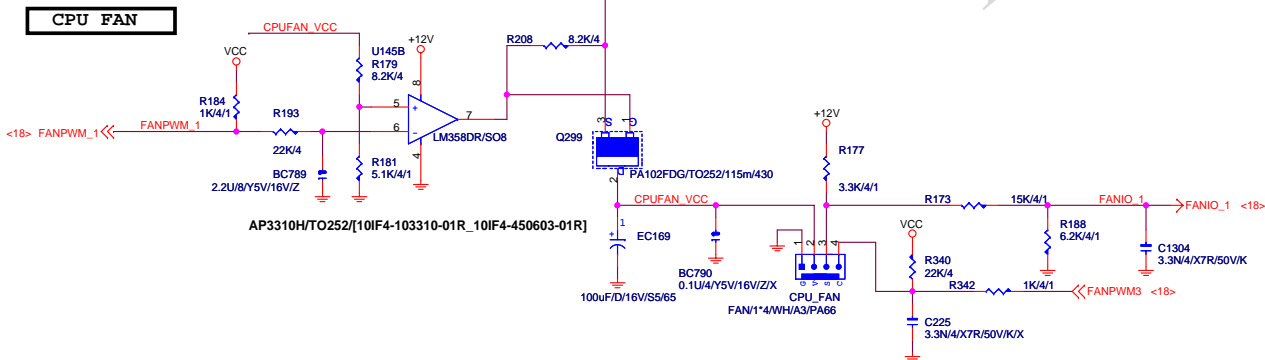
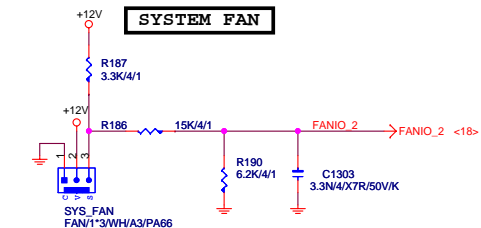
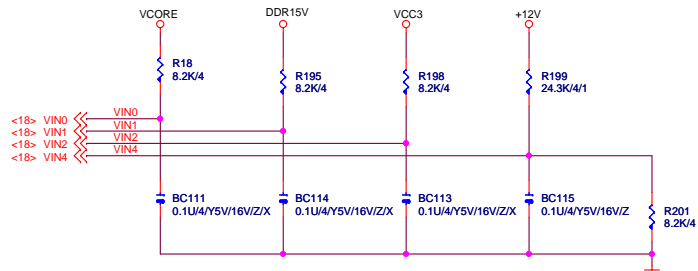
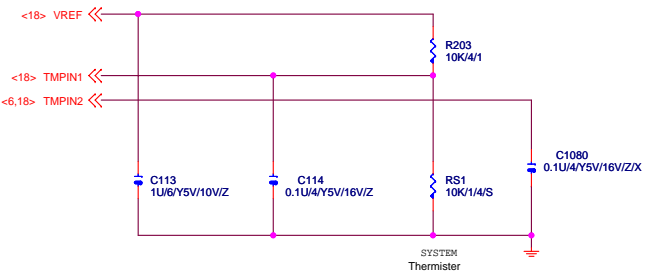
GIGABYTE

ITE 8720

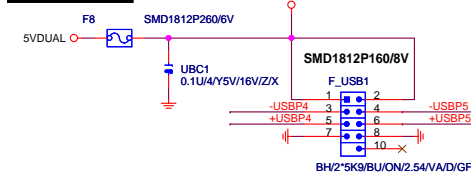
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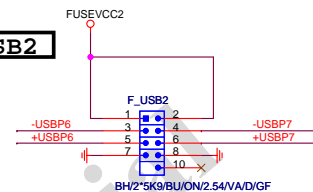
Hardware Monitor circuits



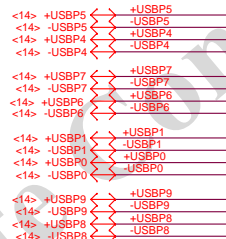
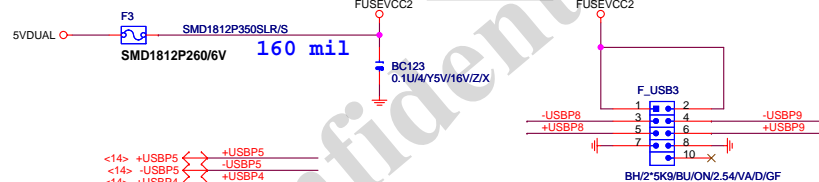
F USB1



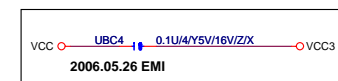
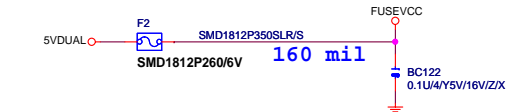
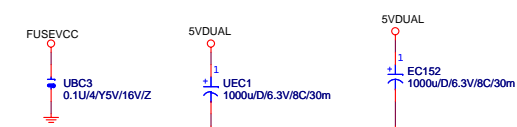
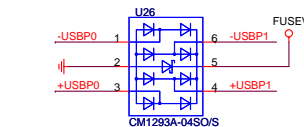
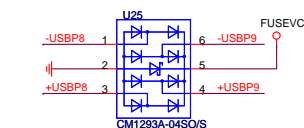
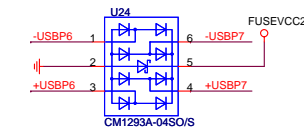
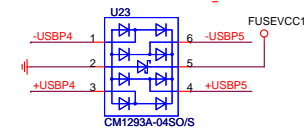
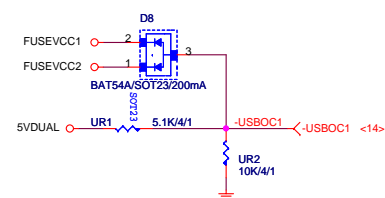
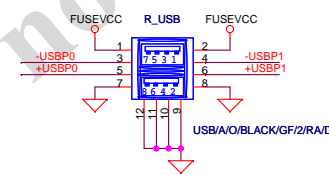
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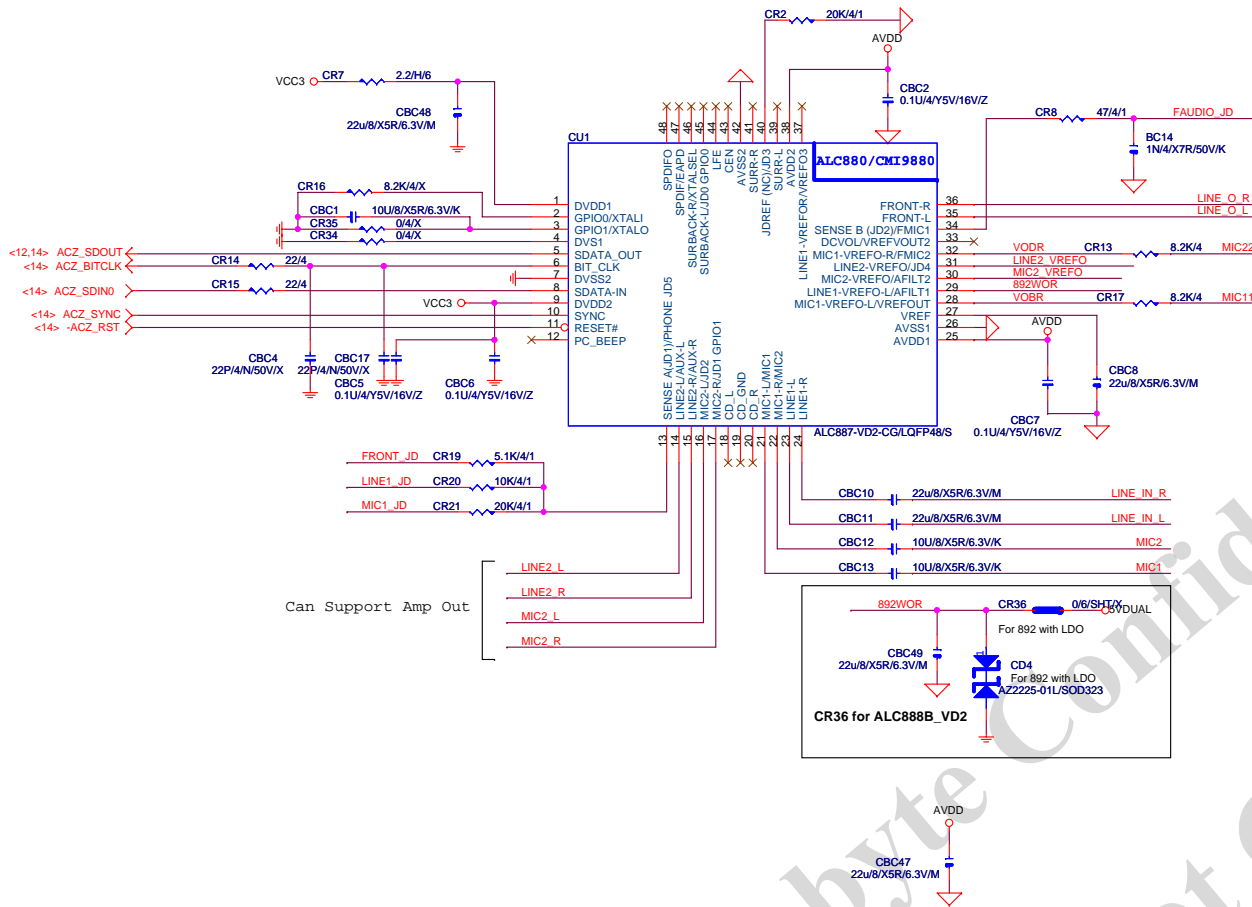
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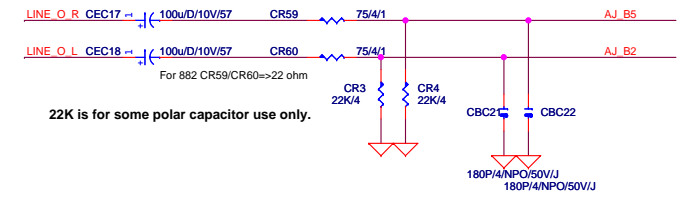
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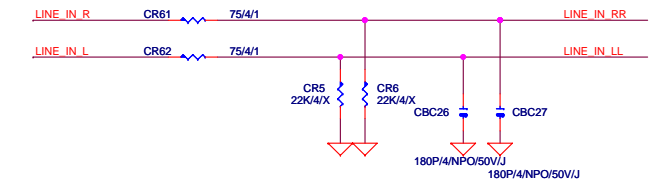
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FANHWMO KB/MS			
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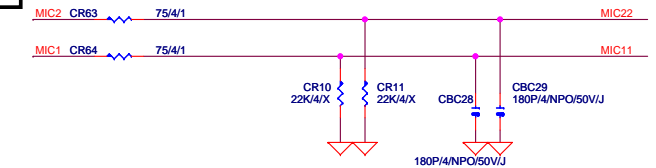
LINE OUT FRONT OUT



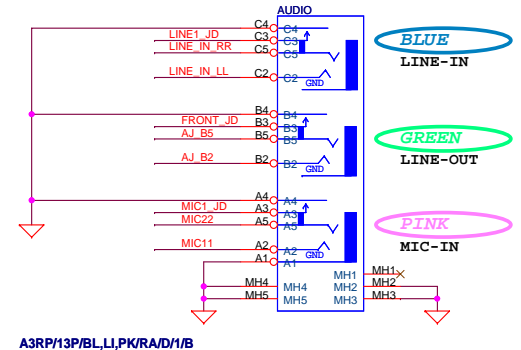
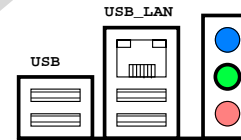
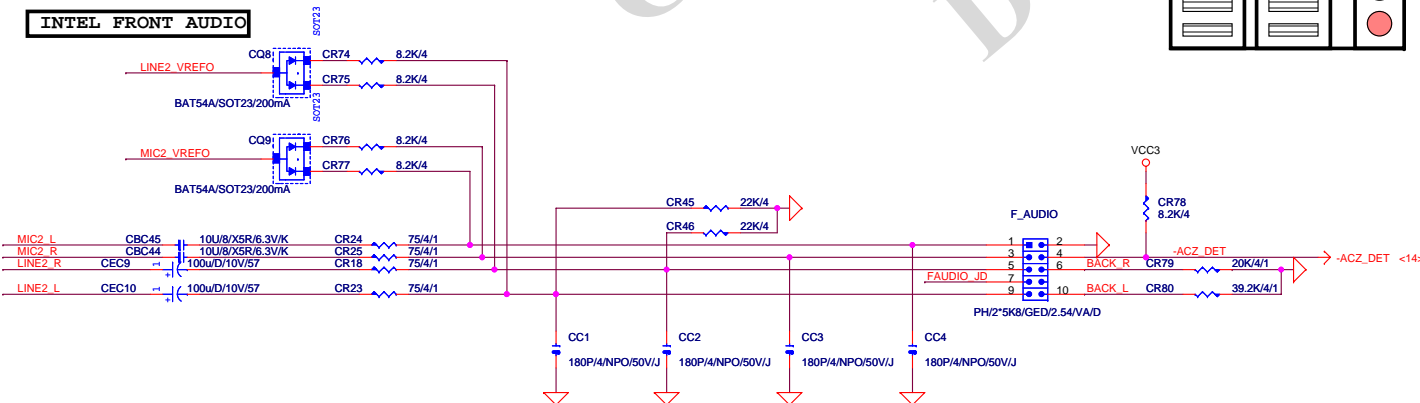
LINE-IN



MIC



INTEL FRONT AUDIO



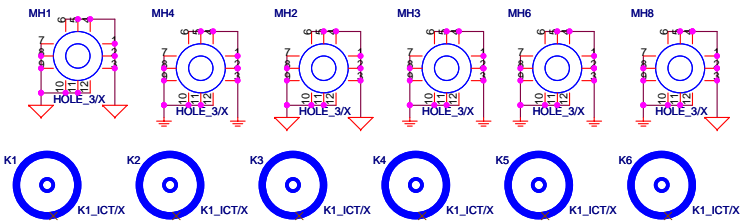
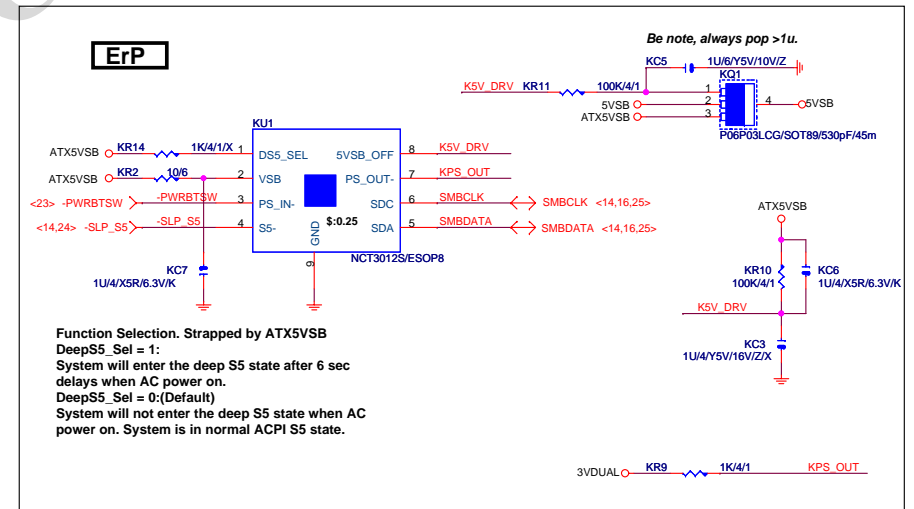
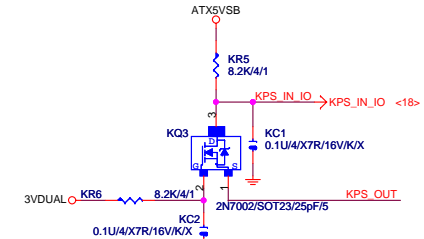
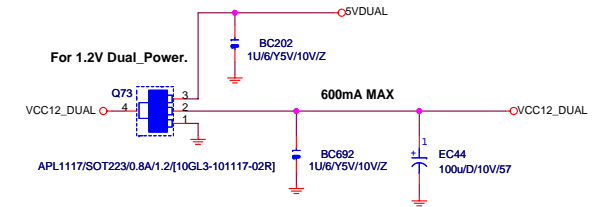
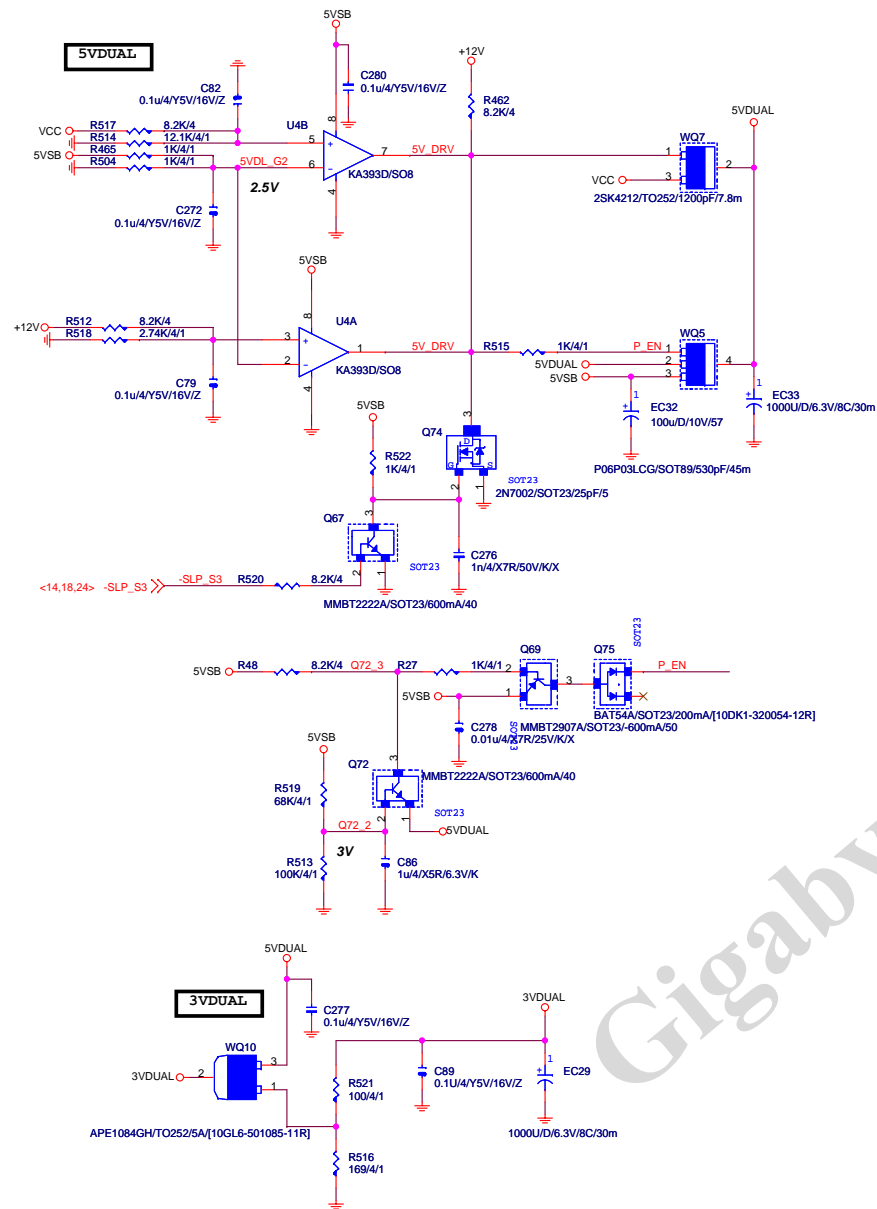
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GIGABYTE

ALC887

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GIGABYTE			
Title			
AUDIO JACK			
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